

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

HARTMUT RUELKE

JOERG HOHAGE

THOMAS WERNER

MICHAEL KIENE

Group Art Unit: Unknown

Examiner: Unknown

Att'y Docket: 2000.108700/DE0363

Customer No.: 23720

Serial No.: Unknown

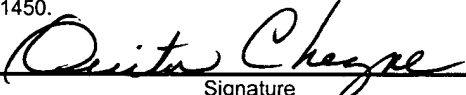
Filed: Concurrently Herewith

For: NITROGEN-ENRICHED LOW-K
BARRIER LAYER FOR A COPPER
METALLIZATION LAYER

SUBMISSION OF PRIORITY DOCUMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

EXPRESS MAIL RECEIPT	
NUMBER:	EV 336536054 US
DATE OF DEPOSIT:	November 19, 2003
I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
	
Signature	

Transmitted for filing herewith is the certified copy of the priority document – German Patent Application No. 103 19 136.4 filed on April 28, 2003.

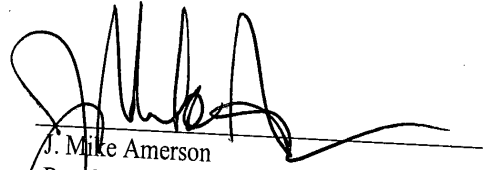
If any fees under 37 C.F.R. §§ 1.16 to 1.21 are required for any reason relating to the enclosed materials, the Assistant Commissioner is authorized to deduct said fees from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/DE0363.

Please date stamp and return the accompanying postcard to evidence receipt of this document.

Respectfully submitted,

WILLIAMS, MORGAN & AMERSON
CUSTOMER NO. 23720

Date: November 19, 2003

A handwritten signature in black ink, appearing to read "J. Mike Amerson", written over a horizontal line.

J. Mike Amerson
Reg. No. 35,426
10333 Richmond, Suite 1100
Houston, Texas 77042
(713) 934-4055
(713) 934-7011 (facsimile)

ATTORNEY FOR APPLICANTS

GRÜNECKER KINKELDEY STOCKMAIR & SCHWANHÄUSSER

ANWALTSSOZIELTÄT

GKS & S MAXIMILIANSTRASSE 58 D-80538 MÜNCHEN GERMANY

RECHTSANWÄLTE LAWYERS

MÜNCHEN
DR. HELMUT EICHMANN
GERHARD BARTH
DR. ULRICH BLUMENRÖDER, LL.M.
CHRISTA NIKLAS-FALTER
DR. MAXIMILIAN KINKELDEY, LL.M.
DR. KARSTEN BRANDT
ANJA FRANKE, LL.M.
UTE STEPHANI
DR. BERND ALLEKOTTE, LL.M.
DR. ELVIRA PFRANG, LL.M.
KARIN LOCHNER
BABETT ERTLE
CHRISTINE NEUHIERL
SABINE PRÜCKNER

PATENTANWÄLTE EUROPEAN PATENT ATTORNEYS

MÜNCHEN
DR. HERMANN KINKELDEY
PETER H. JAKOB
WOLFHARD MEISTER
HANS HILGERS
DR. HENNING MEYER-PLATH
ANNELIE EHNOLD
THOMAS SCHUSTER
DR. KLARA GOLDBACH
MARTIN AUFENANGER
GOTTFRIED KLITZSCH
DR. HEIKE VOGELANG-WENKE
REINHARD KNAUER
DIETMAR KUHLE
DR. FRANZ-JOSEF ZIMMER
BETTINA K. REICHELT
DR. ANTON K. PFAU
DR. UDO WEIGELT
RAINER BERTRAM
JENS KOCH, M.S. (U of PA) M.S.
BERND ROTHAEHEL
DR. DANIELA KINKELDEY
THOMAS W. LAUBENTHAL
DR. ANDREAS KAYSER
DR. JENS HAMMER
DR. THOMAS EICKELKAMP
JOCHEN KILCHERT
DR. THOMAS FRIEDE

PATENTANWÄLTE EUROPEAN PATENT ATTORNEYS

BERLIN
PROF. DR. MANFRED BÖNING
DR. PATRICK ERK, M.S. (MIT)
KÖLN
DR. MARTIN DROPMANN
CHEMNITZ
MANFRED SCHNEIDER

OF COUNSEL PATENTANWÄLTE

AUGUST GRÜNECKER
DR. GUNTER BEZOLD
DR. WALTER LANGHOFF

DR. WILFRIED STOCKMAIR
(-1996)

IHR ZEICHEN / YOUR REF.

UNSER ZEICHEN / OUR REF.

P 35163-04553/we

DATUM / DATE

28.04.03

Applicant: ADVANCED MICRO DEVICES, INC.

One AMD Place, Mail Stop 68,

Sunnyvale, CA 94088-3453

USA

AN IMPROVED NITROGEN ENRICHED LOW-K BARRIER LAYER FOR A COPPER METALLIZATION LAYER

GRÜNECKER KINKELDEY
STOCKMAIR & SCHWANHÄUSSER
MAXIMILIANSTR. 58
D-80538 MÜNCHEN
GERMANY

TEL. +49 89 21 23 50
FAX (GR 3) +49 89 22 02 87
FAX (GR 4) +49 89 21 86 92 93
<http://www.grunecker.de>
e-mail: postmaster@grunecker.de

DEUTSCHE BANK MÜNCHEN
No. 17 51734
BLZ 700 700 10
SWIFT: DEUT DE MM

BUNDESREPUBLIK DEUTSCHLAND



Prioritätsbescheinigung über die Einreichung einer Patentanmeldung

Aktenzeichen: 103 19 136.4

Anmeldetag: 28. April 2003

Anmelder/Inhaber: Advanced Micro Devices Inc.,
Sunnyvale, Calif./US

Bezeichnung: An improved nitrogen enriched low-k barrier
layer for a copper metallization layer

IPC: H 01 L 21/768

Die angehefteten Stücke sind eine richtige und genaue Wiedergabe der ursprünglichen Unterlagen dieser Patentanmeldung.

München, den 12. August 2003
Deutsches Patent- und Markenamt
Der Präsident
Im Auftrag

A handwritten signature in black ink, appearing to read 'Remus'.

AN IMPROVED NITROGEN ENRICHED LOW-K BARRIER LAYER FOR A COPPER METALLIZATION LAYER

FIELD OF THE PRESENT INVENTION

Generally, the present invention relates to the formation of integrated circuits and more particularly to the formation of metallization layers including highly conductive metals, such as copper, embedded into a dielectric material having low permittivity to enhance device performance

DESCRIPTION OF THE PRIOR ART

In modern integrated circuits minimum feature sizes, such as the channel length of field effect transistors, have reached the deep sub micron range, thereby steadily increasing performance of these circuits in terms of speed and/or power consumption. As the size of the individual circuit elements is significantly reduced, thereby improving for example the switching speed of the transistor elements, the available floor space for interconnect lines electrically connecting the individual circuit elements is also decreased. Consequently, the dimensions of these interconnect lines have to be reduced to compensate for a reduced amount of available floor space and for an increased number of circuit elements provided per chip.

In integrated circuits having minimum dimensions of approximately 0.35 micrometer and less a limiting factor of device performance is the signal propagation delay caused by the switching speed of the transistor elements. As the channel length of these transistor elements has now reached 0.18 micrometer and less, it turns out, however, that the signal propagation delay is no longer limited by the field effect transistors but is limited, owing to the increased circuit density, by the close proximity of the interconnect lines, since the line-to-line capacitance is increased in combination with a reduced conductivity of the lines due to their reduced cross-sectional area. The parasitic RC time constants therefore require the introduction of a new type of materials for forming the metallization layer.

Traditionally, metallization layers are formed by a dielectric layer stack including, for example, silicon dioxide and/or silicon nitride with aluminum as the typical metal. Since aluminum exhibits significant electromigration at higher current densities that may be necessary in integrated circuits having extremely scaled feature sizes, aluminum is being replaced by copper, which has a significantly lower electrical resistance and a higher resistivity against electromigration. For devices having feature sizes of 0.13 micrometers and less, it turns out that simply replacing aluminum by copper does not provide for the required decrease of the parasitic RC time constants, and therefore the well established and well known dielectric materials silicon dioxide ($k \approx 4.2$) and silicon nitride ($k > 5$) are increasingly replaced by so-called low-k dielectric materials. However, the transition from the well-known and well established aluminum/silicon dioxide metallization layer to a low-k dielectric/copper metallization layer is associated with a plurality of issues to be dealt with.

For example, copper may not be deposited in relatively high amounts in an efficient manner by well established deposition methods, such as chemical and physical vapor deposition. Moreover, copper may not efficiently be patterned by well established anisotropic etch processes. Therefore the so-called damascene technique is frequently employed in forming metallization layers including copper lines. Typically, in the damascene technique the dielectric layer is deposited and then patterned with trenches and vias that are subsequently filled with copper by plating methods, such as electroplating or electroless plating. Although the damascene technique is presently a well established technique for forming copper metallization layers in standard dielectric materials, such as silicon dioxide, the employment of low-k dielectrics, however, requires the development of new dielectric diffusion barrier layers so as to avoid copper contamination of adjacent material layers, as copper readily diffuses in a plurality of dielectrics. Although silicon nitride is known as an effective copper diffusion barrier, silicon nitride may not be considered as an option in low-k dielectric layer stacks owing to its high permittivity. Therefore, presently silicon carbide is deemed as a viable candidate for a copper diffusion barrier. It turns out, however, that copper's resistance against electromigration strongly depends on the interface between the copper and

the adjacent diffusion barrier layer. Therefore in sophisticated integrated circuits featuring high current densities, it is generally preferable to use up to 20% nitrogen in the silicon carbide layer, thereby remarkably improving the electromigration behaviour of copper compared to pure silicon carbide.

A further problem in forming low-k copper metallization layers has been underestimated in the past and is now considered a major challenge in the integration of low-k dielectrics. During the patterning of the low-k dielectric material, standard photolithography is used to image the required structure into the photoresist that is sensitive in the deep UV range. In developing the photoresist certain portions of the resist, which have been exposed, may however not be completely removed as required and thus the structure may then not be correctly transferred into the underlying low-k dielectric material during the subsequent etch process. The effect of insufficiently developing the photoresist is also referred to as resist poisoning. With reference to Figs. 1a – 1e, a typical conventional process flow will now be described to explain the problems involved in forming a metallization layer including copper and a low-k dielectric in more detail.

Fig. 1a schematically shows a cross-sectional view of a semiconductor structure 100, in which a low-k dielectric material is to be patterned in accordance with a so-called "via first/trench last" process sequence, which is presently considered as the most promising process scheme in patterning low-k dielectrics. The semiconductor structure 100 comprises a substrate 101 that may include circuit elements, such as transistors, resistors, capacitors, and the like, and which may include a lower metallization layer 102 including a metal region 103 embedded in a dielectric material 104. Depending on the level of the lower metallization layer 102, the metal region 103 may comprise copper and the dielectric 104 may be a low-k dielectric, such as hydrogen containing silicon oxycarbide (SiCOH). A barrier layer 105 formed of nitrogen containing silicon carbide (SiCN) which also serves as an etch stop layer in the following etch procedure for patterning an overlying low-k dielectric layer 106. The low-k dielectric layer 106 may comprise, depending on the process sequence used, an intermediate etch stop layer 107, which in many applications may, however, be omitted for the benefit of a reduced total permittivity. The low-k dielectric material in the layer 106 may comprise SiCOH. A cap layer 108, for

example comprised of oxide or provided as an antireflective coating (ARC), may optionally be located on the low-k dielectric layer 106 and may then serve as a stop layer in removing excess copper in a subsequent chemical mechanical polishing process (CMP). A resist mask 109 including an opening 110 is formed above the optional cap layer 108.

A typical process flow for forming the semiconductor structure 100 as shown in Fig. 1a may comprise the following steps. After planarizing the lower metallization layer 102, the barrier/etch stop layer 105 is deposited, for example by a plasma enhanced chemical vapour deposition (PECVD) from trimethyl silane (3MS) and ammonia (NH_3) as precursor gases. Then, the hydrogen containing silicon oxycarbide 104 is deposited, wherein, if required, the silicon carbide layer 107 is formed when a first adequate thickness of the dielectric layer 106 is obtained. Thereafter, the residual layer 106 is deposited to achieve the required overall thickness of the layer 106. Next, the cap layer 108, if required, is deposited with a desired thickness. The cap layer 108 may help to substantially avoid any interaction of the low-k dielectric of the layer 106 with the overlying resist mask 109 and may serve as a CMP stop layer. Then the resist mask 109 is patterned in accordance with well established deep-UV lithography techniques to form the opening 110 determining the dimensions of the vias to be formed within the dielectric layer 106.

Fig. 1b schematically shows the semiconductor structure 100 after an anisotropic etch process for forming a via 111 in the cap layer 108 and the dielectric layer 106. During the anisotropic etch procedure the barrier/etch stop layer 105 exhibits a significantly lower etch rate than the surrounding dielectric layer 106, so that the etch process may be stopped in or on the layer 105. Thereafter, the remaining photoresist not consumed during the anisotropic etch process is removed by an etch step in an oxygen-containing plasma ambient. It should be noted, that in particular the nitrogen contained in the barrier/etch stop layer 105 may readily diffuse into the low-k dielectric of the layer 106 due to the desired porosity of this material. Since the cap layer 108 substantially prevents any diffusion from nitrogen or nitrogen-containing compounds into the overlying resist mask 109, the patterning

of the opening 110 and the subsequent patterning of the via 111 is substantially not affected by any resist poisoning effects.

Fig. 1c schematically shows the semiconductor structure 100 in an advanced manufacturing stage. The via 111 is filled with an organic antireflective coating material so as to include a via plug 114, whereas the organic material is provided at the remaining surface of the structure 100 so as to form an antireflective coating layer 112 for the subsequent photolithography. Thus, the plug 114 and the antireflective coating 112 serve to planarize the topography of the semiconductor structure 100 prior to the formation of a further photoresist mask 113. As shown, the photoresist mask 113 includes a trench opening 115 at the bottom of which resist residuals 116 are maintained.

The via plug 114 and the antireflective coating 112 may be formed by spin-on techniques, and the like, and the photoresist mask 113 may be formed by sophisticated lithography methods, as are well known in the art. Contrary to the formation of the resist mask 109, nitrogen or nitrogen compounds that may originate from the layer 105 may readily diffuse in the organic antireflective coating material and may now come into contact with the overlying photoresist 113, since the protecting cap layer 108 is open at the via 111. The interaction of nitrogen and compounds thereof with the photoresist may deteriorate the light sensitivity of the resist. Consequently, upon exposure and development of the photoresist 113 in forming the trench opening 115, the resist residuals 116 remain and significantly affect the following anisotropic etch step for forming a trench in the upper portion of the dielectric layer 106.

Fig. 1d schematically shows the semiconductor structure 100 after completion of the trench forming step. As is evident from Fig. 1d, the trench 117 that should have been formed in the dielectric layer 106 is substantially not transferred from the photoresist mask 113 to the underlying cap layer 108 and the upper portion of the dielectric layer 106. Thus, after removing the remaining photo resist mask 113 the cap layer 108 and the dielectric layer 106 comprise substantially the via 111 without any trench in the upper portion of the layer 106. Even a significant increase of the thickness of the antireflective coating 112 may not efficiently prevent the overlying

photoresist layer 113 from interacting with up-diffusing nitrogen containing compounds.

Fig. 1e schematically shows the semiconductor structure 100 after completion of the metallization layer 130 including a barrier metal layer 118 on inner side walls and the bottom of the via 111, which is filled with copper 119. Moreover, a surface 120 of the metallization layer 130 is planarized to allow the formation of a further metallization layer.

Typically, the barrier metal layer 118 may be deposited by physical vapour deposition, such as sputter deposition with a thickness that insures sufficient protection against copper out diffusion and at the same time provides for a required adhesion to the surrounding low-k dielectric material. For example, tantalum and/or tantalum nitride may be used as material for the barrier metal layer 118. Subsequently, a copper seed layer is deposited to promote the subsequent deposition of the bulk copper by electroplating. Then, the excess copper is removed by chemical mechanical polishing, wherein the cap layer 108 is also removed and acts as a stop layer, to reliably control the CMP process. However, since the trenches 117 required for the electrical connection are missing, as shown in Fig. 1d and 1e, or are at least substantially reduced in size, device failures occur or at least a significantly reduced device reliability is caused. Moreover, as electromigration of copper strongly depends on the characteristics of the interface to the surrounding material, it is important to maintain a required nitrogen concentration within the layer 105, especially at regions 121, in which the copper of the metal region 103 is in contact with the barrier/etch stop layer 105, so as to obtain the required electromigration behaviour, an improved adhesion, and the like, compared to pure silicon carbide layers.

In view of the above problems, it is thus highly desirable to provide a technique that provides superior barrier characteristics without unduly promoting resist poisoning in the formation of low-k metallization layers.

SUMMARY OF THE INVENTION

Generally, the present invention is directed at a method and a device to provide the required nitrogen concentration in a dielectric barrier/etch stop layer that may comprise silicon carbide, wherein a surface of the layer is modified by plasma treatment so as to significantly reduce the nitrogen migration therethrough while maintaining the desired barrier characteristics.

According to one illustrative embodiment of the present invention a method comprises forming a nitrogen enriched silicon carbide-containing layer over a substrate. Moreover, at least a surface of the nitrogen enriched silicon carbide-containing layer is modified by treating the same with an inert plasma atmosphere.

According to another illustrative embodiment of the present invention a method of forming a metallization layer comprises depositing a nitrogen-containing low-k barrier layer over a substrate and modifying a surface of the nitrogen-containing low-k barrier layer by a plasma treatment. Then, a low-k dielectric layer is deposited over the low-k barrier layer and the low-k dielectric layer is patterned by a lithography process, wherein the modified surface reduces resist poisoning during the lithography process. Finally, a metal region is formed in the patterned low-k dielectric layer.

According to still another illustrative embodiment of the present invention, a semiconductor device comprises a substrate and a metallization layer formed above the substrate. The metallization layer includes a dielectric barrier layer comprising silicon carbide and nitrogen, wherein the dielectric barrier layer has a first surface and a second surface. A noble gas atom concentration at the first surface is higher than at the second surface. The metallization layer further includes a low-k dielectric layer having formed therein a metal region, wherein the first surface is in contact with the low-k dielectric layer.

According to still a further embodiment of the present invention a method, comprises forming a barrier layer comprised of a nitrogen-enriched silicon carbide-containing layer over a substrate. A first surface of the barrier layer is exposed to a

plasma ambient comprising a noble gas to thereby increase a concentration of atoms of said noble gas in a first region of said barrier layer having a first depth. Then, at least one dielectric layer is formed above the barrier layer after the first surface of the barrier layer is exposed to the plasma ambient and a conductive interconnection is formed in the at least one dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Further advantages, objects and embodiments of the present invention are defined in the appended claims and will become more apparent with the following detailed description when taken with reference to the accompanying drawings, in which:

Figs. 1a – 1e schematically show cross-sectional views of a semiconductor structure including a low-k metallization layer, wherein trenches in the low-k dielectric are substantially not formed owing to resist poisoning in the dual damascene process; and

Figs. 2a – 2f schematically show cross-sectional views of a semiconductor structure during various stages in manufacturing a low-k metallization layer with reduced resist poisoning according to illustrative embodiments of the present invention.

DETAILED DESCRIPTION

While the present invention is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present invention to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present invention, the scope of which is defined by the appended claims.

The present invention is based on investigations the inventors have performed in order to clarify the reasons for resist poisoning in a typical dual damascene process

sequence. It is believed that a reaction of amine species, that is, nitrogen hydrogen compounds (N-H^*), created by diffusion of nitrogen into the overlying low-k dielectric interact with the low-k dielectric and, upon up-diffusion, with the photoresist. The interaction of the nitrogen-containing compounds with the photoresist may then lead to undeveloped resist residuals in the trench resist mask in a via first/trench last process. According to the present invention, the nitrogen contained in the barrier/etch stop layer (for convenience the term "barrier layer" will be used hereinafter) or in any other material regions provided below the barrier layer is substantially confined by modifying the surface of the barrier layer, thereby maintaining the superior barrier and adhesion characteristics to an underlying metal. The surface modification may be accomplished by a plasma treatment after the deposition of the barrier layer, wherein an in-situ deposition and plasma treatment scheme may be advantageous in view of tool utilization and throughput. The term in-situ is to be understood as a process sequence requiring the establishment of one or more atmospheres in a vacuum, that is, negative pressure, ambient, wherein the vacuum is substantially maintained during each process of the sequence, or in other words, wherein the substrate is not exposed to the ambient atmosphere prevailing outside of a process tool or process chamber.

With reference to Figs. 2a – 2j further illustrative embodiments of the present invention will now be described.

In Fig. 2a a semiconductor structure 200 comprises a substrate 201 over which a first metallization layer 202 is formed. As already explained with reference to Figs. 1a – 1e, the substrate 201 may include any circuit elements, such as transistors, resistors, capacitors, and the like, wherein the first metallization layer 202 provides electrical contact to at least some of the circuit elements. The first metallization layer 202 may represent the very first metallization layer or may represent any intermediate metallization layer over which one or more additional metallization layers are to be formed. The first metallization layer 202 may include a first dielectric layer 204 with a first metal region 203 contained therein. In the present example, the first metal region 203 may be comprised of copper including a barrier diffusion layer (not shown) provided between the dielectric material 204 and the copper of the first metal region 203. A barrier layer 250 is formed over the first

metallization layer 202 and has a first surface 251 and a second surface 252 in contact with the first metallization layer 202. In one particular embodiment, the barrier layer 250 is comprised of silicon carbide that contains an enhanced concentration of nitrogen for the required barrier and adhesion characteristics. For example, the nitrogen concentration may be in the range of approximately 20 to 30 weight percent. A surface region including the surface 251 of the barrier layer 250 has a modified structure compared to lower lying portions of the barrier layer 250. For instance, the surface 251 and portions up to a depth of about 2 to 30 Angstrom may have an increased density compared to the residual barrier layer 250, wherein additional inert atoms, such as argon, krypton or other noble gas atoms, are incorporated into the barrier layer 250. In one particular embodiment, helium atoms may be present in the barrier layer 250 in addition to silicon, carbon and nitrogen. In this respect it is to be noted that other impurities may be present in the barrier layer 250 depending on the "process history" for forming the barrier layer 250. However, these impurities are incorporated in a significant lesser amount than silicon, carbon, nitrogen and the inert component, such as helium. Although some of these impurities may also contribute to resist poisoning in a conventional structure, such as the one described with reference to Fig. 1a to 1e, the modified surface 251 significantly reduces the diffusion activity of these impurities and also the diffusion of nitrogen, thereby effectively decreasing the amount of nitrogen compounds that may diffuse from the barrier layer 250 and lead to resist poisoning in further manufacturing processes, as will be described later.

A typical process flow for manufacturing the semiconductor structure 200, as shown in Fig. 2a may include the following steps. First, the substrate 201 may be provided having already formed thereon the first metallization layer 202. The formation of the first metallization layer 202 may comprise substantially the same steps as used for the formation of a subsequent metallization layer as will be described in more detail later in this application and thus description thereof will be omitted here. Thereafter, the barrier layer 250 is deposited by, for example, plasma enhanced CVD with a required thickness, for example in the range of approximately 10 – 100 nanometer. During deposition, the amount of a nitrogen-containing precursor gas may be controlled so as to obtain nitrogen concentration in the deposition ambient

and thus in the deposited layer 250 as is required for the desired barrier and adhesion characteristics.

In one embodiment, precursor gases 3MS (trimethyl silane) and ammonia (NH_3), 4MS (tetramethyl silane), liquid precursors, such as TOMCAT™, OMCTS, and the like, are used in combination with an inert gas, such as helium, to establish a reactive ambient for the deposition of a nitrogen-containing silicon carbide layer. The ratio between 3MS and ammonia (NH_3) substantially determines the amount of nitrogen incorporated into the silicon carbide layer 250. The deposition may take place in any appropriate CVD process tool (not shown), which additionally allows the establishment of a plasma ambient. For example, plasma enhanced CVD deposition systems available from Applied Materials such as DXZ™ or Producer™ may be used. For the above specified deposition tool typical process parameters may be as follows:

gas flows: 3MS: about 100 to 200, for example 160 sccm;
ammonia (NH_3): about 200 to 500, for example 325 sccm;
He: about 350 to 450, for example 400 sccm;
HF power: about 200 to 400 Watt, for example 300 Watt;
pressure: about 2 to 4 Torr, for example 3 Torr;
substrate temperature: about 300 to 400 °C, for example 335°C;

For the above specified parameters and a deposition time of about 15 to 20 seconds a thickness of the barrier layer may be obtained in the range of approximately 20 to 70 nanometers (nm). The nitrogen concentration of the barrier layer may range from approximately 20-30 weight percent. The above parameter ranges as well as the specified precursor and carrier gases may provide sufficient guidance for the skilled person so as to readily adapt the process to the actually used deposition tool and deposition scheme.

In Fig. 2b the semiconductor structure 200 is depicted after the deposition of the barrier layer 250, when exposed to a plasma atmosphere 260 for modifying the surface 251. In one particular embodiment, the plasma atmosphere 260 may be established from a noble gas, e.g., a helium gas atmosphere. The helium plasma

atmosphere 260 enables the modification of the structure of the surface 251 and a region adjust the surface 251 without substantially deteriorating the characteristics of the remaining portion of the barrier layer 250 due to the light atomic weight of the helium particles. Thus, a region of only a few Angstrom (e.g., 3 - 30Å) thickness below the surface 251 may be affected by the plasma atmosphere 260, while nevertheless effectively densifying the surface 251 to thereby significantly reducing nitrogen migration therethrough. That is, by exposing the surface 251 of the barrier layer 250 to the plasma ambient, the concentration of helium atoms (or other noble gas atoms) is increased relative to the concentration of such noble gas atoms in the remainder of the barrier layer 250. The depth of the region exhibiting an increased concentration of noble gas atoms may vary depending on the particular application. In one illustrative embodiment, the depth of such a region may be approximately 0.3 -3 nm. In other embodiments, heavier inert particles, such as argon particles, may be used in establishing the plasma atmosphere 260, when a more significant impact on portions located more deeply is tolerable.

In one particular embodiment, the deposition of the barrier layer 250 and the treatment with the plasma atmosphere 260 are performed as an in-situ sequence, thereby optimizing tool utilization and throughput. For instance, the above identified deposition tools or any other appropriate deposition tool may be used with process parameters for the plasma atmosphere 260 as follows.

gas flow: He: about 1500 to 4000 sccm, for example 2600 sccm;
HF power: about 200 to 500 Watt, for example 350 Watt;
pressure: about 7.0 to 10 Torr, for example 8.7 Torr;
substrate temperature: about 300 to 400 °C, for example 335 °C.

A time interval for the plasma treatment may range from approximately 10 – 60 seconds.

It may be appreciated that the process parameters of the plasma atmosphere 260 may mutually depend from each other as well as on the specifics of the process chamber of the deposition tool, such as the geometry of the chamber, the configuration and equipment of the process chamber, and the like. Starting with the

above specified values, however, a suitable set of parameter values may be obtained for any type of deposition tool by experiment.

In one embodiment, the plasma treatment may be preceded by a purge step so as to remove precursor gases and/or reaction byproducts created during the deposition of the barrier layer 250. To this end, the supply of the precursors, such as 3MS and ammonia (NH_3) may be discontinued and a purge gas may be fed to the process chamber. In one embodiment, the purge gas may be the same as is used in establishing the plasma atmosphere 260. Typically, the duration of the purge step may range from about 3 to 10 seconds. However, in some cases it may be considered appropriate to prolong the purge step beyond the above specified time intervals to minimize traces of impurities, whereas in other cases the purge step may be omitted or may be combined with a stabilizing step for establishing a gaseous atmosphere prior to igniting a plasma. For instance, a gaseous atmosphere including a gas as is used for the plasma atmosphere 260, such as helium, may be generated for an appropriate time period with a pressure that is suitable for creating the plasma atmosphere 260, wherein a part of the stabilizing step may be used to remove undesired contaminants, such as nitrogen. Typically, stabilizing step may range from about 5 to 15 seconds, for example about 12 seconds.

In other embodiments, heavier inert atoms may be used in establishing the plasma atmosphere 260, when the impact of the heavier particles on the barrier layer 250 may be tolerable. For instance, argon, krypton or other noble gases may be used to modify the surface 251 by releasing among others nitrogen and/or by incorporating these heavier particles into the barrier layer 250, thereby reducing the release and thus the diffusion of nitrogen in subsequent processes as will be described in more detail below.

Fig. 2c schematically shows the semiconductor structure 200 in an advanced manufacturing stage similar to that shown in Fig. 1a. Thus, the semiconductor structure 200 comprises a low-k dielectric layer 206 that may be comprised of a first layer and a second layer with an etch stop layer 207, for example formed of silicon carbide, interposed therebetween, whereas in other embodiments the etch stop

layer 207 is omitted. The low-k dielectric layer 206 is comprised of any appropriate dielectric material, such as silicon oxycarbide (SiCOH), and the like. A cap layer 208 may optionally be formed over the dielectric layer 206 and a resist mask 209 having formed therein an opening 210 is formed over the cap layer 208.

Regarding the formation of the semiconductor structure 200 as shown in Fig. 2c, the same processes may be employed as previously explained with reference to Fig. 1a. It should be noted, however, that due to the reduced release and interdiffusion of nitrogen and compounds thereof at the modified surface 251, the diffusion of nitrogen into the overlying low-k dielectric is significantly lower than in the corresponding prior art process flow. Thus, the dielectric layer 206 comprises only a minimum amount of nitrogen and nitrogen compounds. As a consequence, even in the absence of the cap layer 208 resist poisoning of the resist mask 209 is significantly reduced.

Fig. 2d shows the semiconductor structure 200 after the anisotropic etch procedure for forming a via 211 in the (optional) cap layer 208, the dielectric layer 206, the optional etch stop layer 207 and partially in the barrier layer 250 acting as an etch stop layer, thereby leaving a thickness 255 after the etch process. In one embodiment, the modification of the surface 251 may substantially reach down to the remaining portion of the barrier layer 250 having the thickness 255. In this way liberation of nitrogen during the etch process or in a subsequent fill process is suppressed. A corresponding "depth" of the modified portion may be accomplished by appropriately adjusting the conditions during the treatment with the plasma atmosphere 260. For instance, the treatment time and/or the substrate temperature and/or the pressure and/or the type of plasma particles may be correspondingly selected so as to achieve the desired depth in modifying the surface 251.

In other embodiments, after etching the via 211 a subsequent step for out-gassing contaminants from exposed portions of the barrier layer 250 may be performed, possibly at an elevated temperature, to remove the contaminants prior to the following lithography processes. During the out-gassing the modified surface 251 restricts the diffusion of nitrogen and nitrogen compounds of non-exposed portions of the barrier layer 250. Thus, even for a modification that is substantially restricted

to the surface 251 of the barrier layer 250, nitrogen contamination in subsequent process steps may be minimized.

Fig. 2e schematically depicts an advanced manufacturing stage, wherein the via 211 is filled with an organic antireflective coating 214 material to form a via plug and a corresponding antireflective layer 212 is formed on the dielectric layer 206. A photoresist mask 213 having a trench opening 215 is formed over the antireflective layer 212.

In forming the opening 215 in the patterned photoresist mask 213 as shown in Fig. 2e, wherein substantially the same process steps may be involved as already described with reference to Fig. 1c, the amounts of nitrogen and nitrogen compounds from the barrier layer 250 diffusing up to the dielectric layer 206 in previous process steps and finally reaching the photoresist mask 213 may be reduced such that resist poisoning is reduced or eliminated. Therefore, the trench opening 215 is substantially completely open and includes only an insignificant amount of resist residuals or is even substantially free of resist residuals.

In other embodiments, the amount of resist residuals may be determined by, for example, optical measurements, the results of which may then be used to assess an "appropriateness" of the resist mask 213 for further processing. On the basis of the appropriateness the substrate 201 may then be rejected or released. A rejection of the substrate 201 may result in a further out-gassing step as described above, wherein the resist mask 213 may be removed prior to or after the out-gassing. In one illustrative embodiment, the measurement results may be used to readjust one or more process parameters, such as process time, for the plasma treatment with the plasma atmosphere 260 and/or of the out-gassing step as described above, to maintain the amount of resist residuals within a specified range.

Fig. 2f shows the semiconductor structure 200 after anisotropically etching the upper portion of the dielectric layer 206 to form a trench 217 that substantially corresponds to the dimensions of the trench opening 215 in the photoresist mask 213. Etching the trench 217 and subsequently removing the antireflective coating

212 and the residual photoresist 213 may be carried out as already described with reference to Fig. 1d. Moreover, the barrier layer 250 may be completely opened to provide a connection to the underlying metal region 203.

Fig. 2g schematically shows the semiconductor structure 200 with a second metallization layer 230 formed over the first metallization layer 202 and partially separated therefrom by the barrier layer 250. Moreover, a barrier metal layer 218 is formed inside the trench opening 217 and the via opening 211, wherein these openings are now filled with copper 219 so that an electrical connection is provided between the first metal region 203 and the trench 217. Moreover, the cap layer 208 is removed so that a substantially planar surface 220 is provided that may receive a further metallization layer, such as the second metallization layer 230.

Regarding the formation of the structure as shown in Fig. 2g the same criteria apply as already pointed out with reference to Fig. 1d. In particular, interface portions 221 of the barrier layer 250 that are in contact with the first metal region 203 exhibit a sufficiently high nitrogen concentration to provide for the required electromigration and adhesion characteristics, whereas at the opposing modified surface 251 the adhesion to the dielectric layer 206 are substantially not negatively affected. This is accomplished by modifying the barrier layer 250 with a plasma treatment after deposition, resulting in an increased noble gas atom concentration at the surface 251 compared to the surface 252 that is in contact with the metallization layer 202.

Further modifications and variations of the present invention will be apparent to those skilled in the art in view of this description. Accordingly, the description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the present invention. It is to be understood that the forms of the invention shown and described herein are to be taken as the presently preferred embodiments.

CLAIMS

1. A method comprising:

forming a nitrogen enriched silicon carbide-containing layer over a substrate; and

modifying at least an exposed surface of the nitrogen enriched silicon carbide-containing layer by treating the exposed surface with an inert plasma atmosphere.

2. The method of claim 1, wherein said plasma atmosphere is established without interrupting a vacuum condition generated during the formation of said nitrogen enriched silicon carbide-containing layer.

3. The method of claim 1, wherein said plasma atmosphere is substantially established from helium.

4. The method of claim 1, wherein said nitrogen enriched silicon carbide-containing layer is formed by plasma enhanced vapor deposition.

5. The method of claim 1, further comprising, prior to modifying the surface, purging said substrate with a gas used to establish said plasma atmosphere.

6. The method of claim 5, further comprising, prior to modifying the surface, establishing a stabilized gaseous atmosphere including a gas used to subsequently establish said plasma atmosphere.

7. The method of claim 1, further comprising forming a low-k dielectric layer over said nitrogen enriched silicon carbide-containing layer, wherein diffusion of contaminants emanating from said nitrogen enriched silicon carbide-containing layer is reduced due to the surface modification.

8. The method of claim 7, further comprising patterning said low-k dielectric layer by photolithography and etching, wherein resist poisoning is reduced by said reduced diffusion of contaminants.

9. The method of claim 8, wherein patterning said low-k dielectric layer includes forming a via in said low-k dielectric layer by means of a first resist mask and forming a trench in an upper portion of said low-k dielectric layer by means of a second resist mask.

10. The method of claim 9, further comprising, prior to forming said trench, performing an out-gassing step to remove contaminants.

11. The method of claim 8, further comprising determining a degree of said resist poisoning.

12. The method of claim 11, further comprising controlling, on the basis of said determined degree, at least one process parameter for treating the surface with said plasma atmosphere.

13. A method of forming a metallization layer, the method comprising:

depositing a nitrogen-containing low-k barrier layer over a substrate;

modifying a surface of said nitrogen-containing low-k barrier layer by introducing noble gas atoms into a region of said barrier layer by exposing said barrier layer to a plasma treatment comprising a noble gas;

depositing a low-k dielectric layer over said low-k barrier layer;

patterning said low-k dielectric layer by a lithography process, wherein said modified surface reduces resist poisoning in said lithography process; and

forming a metal region in said patterned low-k dielectric layer.

14. The method of claim 13, wherein said nitrogen-containing low-k barrier layer comprises silicon carbide.

15. The method of claim 13, wherein depositing said nitrogen-containing low-k barrier and modifying a surface thereof is performed without exposing said substrate to an ambient atmosphere.
16. The method of claim 13, wherein said plasma treatment includes establishing a plasma atmosphere on the basis of a noble gas.
17. The method of claim 16, further comprising stabilizing a gas atmosphere including helium prior to establishing said plasma atmosphere.
18. The method of claim 16, further comprising purging said substrate with a noble gas prior to establishing said plasma atmosphere.
19. The method of claim 13, wherein patterning said low-k dielectric layer includes forming a via in said low-k dielectric layer by means of a first resist mask and forming a trench in an upper portion of said low-k dielectric layer by means of a second resist mask.
20. The method of claim 19, further comprising, prior to forming said trench, performing an out-gassing step to remove contaminants.
21. The method of claim 19, further comprising determining a degree of said resist poisoning.
22. The method of claim 21, further comprising controlling, on the basis of said determined degree, at least one process parameter for said plasma treatment.
23. A semiconductor device comprising:

a substrate;

a metallization layer formed above the substrate, the metallization layer including

a dielectric barrier layer comprising silicon carbide and nitrogen, the dielectric barrier layer having a first surface and a second surface, wherein a noble gas atom concentration at the first surface is higher than at the second surface,

a low-k dielectric layer having formed therein a metal region, wherein said first surface is in contact with said low-k dielectric layer.

24. A method, comprising:

forming a barrier layer comprised of a nitrogen-enriched silicon carbide-containing layer over a substrate;

exposing a first surface of said barrier layer to a plasma ambient comprising a noble gas to thereby increase a concentration of atoms of said noble gas in a first region of said barrier layer having a first depth;

forming at least one dielectric layer above said barrier layer after said first surface of said barrier layer is exposed to said plasma ambient; and

forming a conductive interconnection in said at least one dielectric layer.

25. The method of claim 24, wherein said nitrogen-enriched silicon carbide containing layer is comprised of approximately 10 – 30 weight% nitrogen.

26. The method of claim 24, wherein, said noble gas is comprised of at least one of helium, argon and krypton.

27. The method of claim 24, wherein said first depth ranges from approximately 0.3 - 3 nm.

ABSTRACT

The effect of resist poisoning may be eliminated or at least substantially reduced in the formation of a low-k metallization layer, in that a nitrogen-containing barrier layer is provided with a surface modified by plasma treatment. Consequently, diffusion of nitrogen and nitrogen compounds in vias formed in the low-k dielectric layer is significantly suppressed, so that in a subsequent photolithographic step interaction of nitrogen and nitrogen compounds with the photoresist is remarkably reduced.

1/4

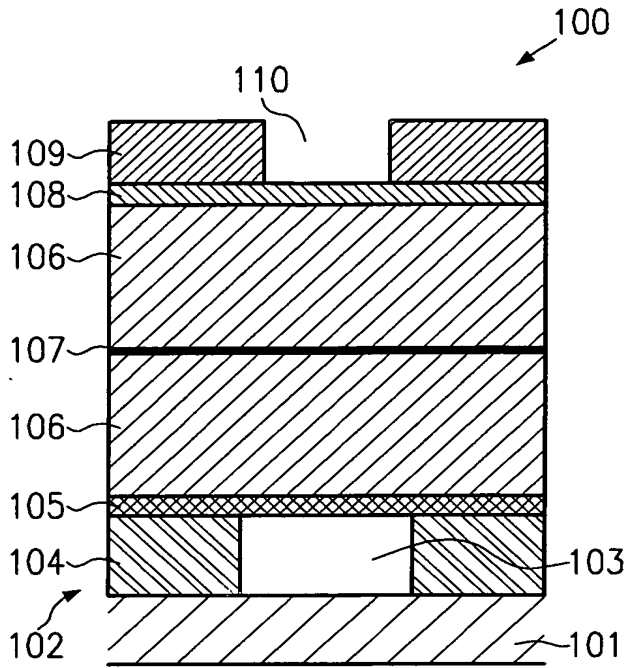


FIG. 1a
(prior art)

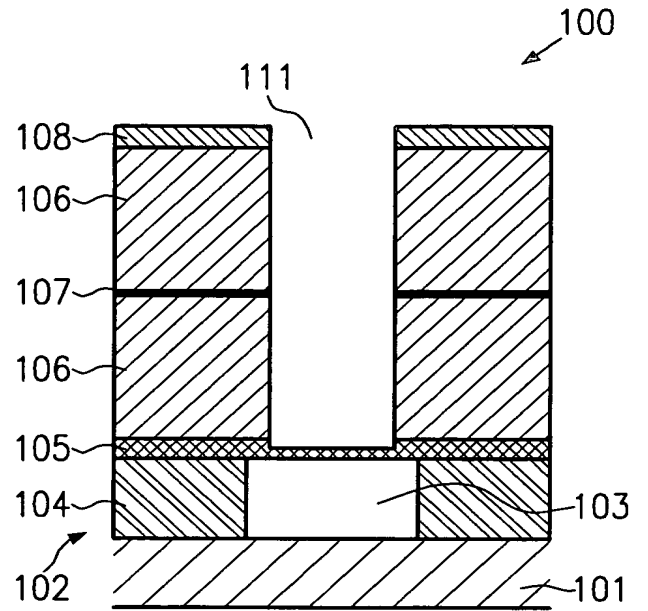


FIG. 1b
(prior art)

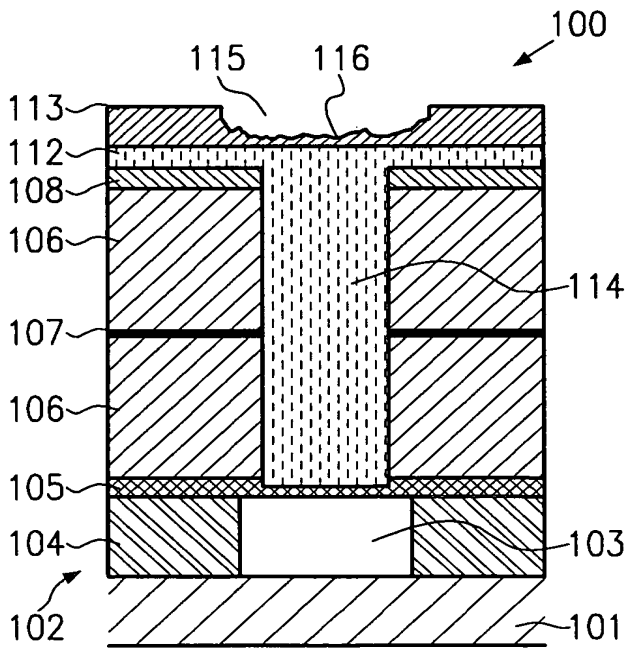


FIG. 1c
(prior art)

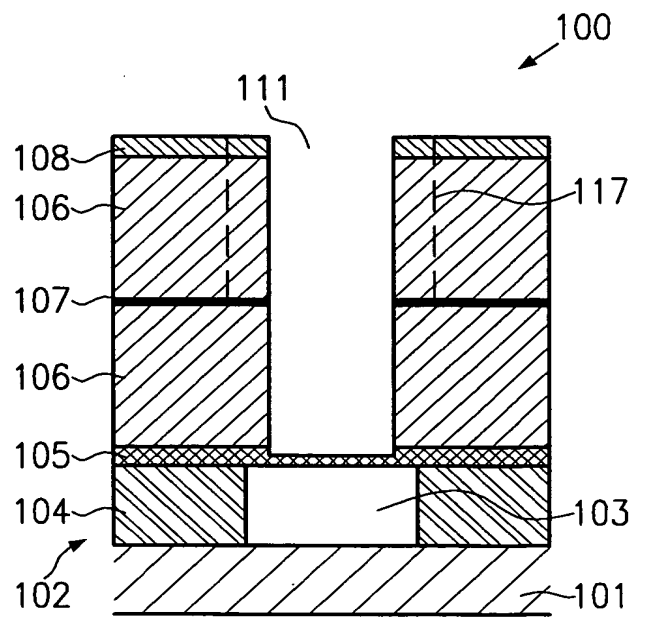


FIG. 1d
(prior art)

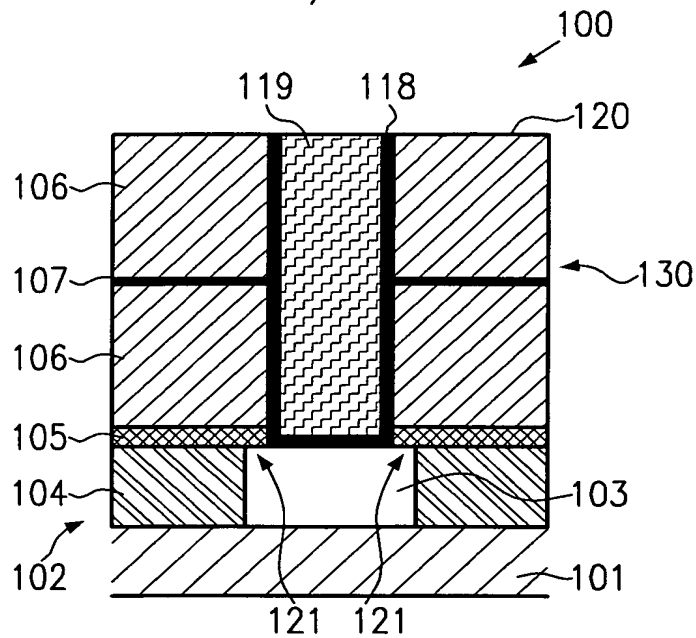


FIG. 1e
(prior art)

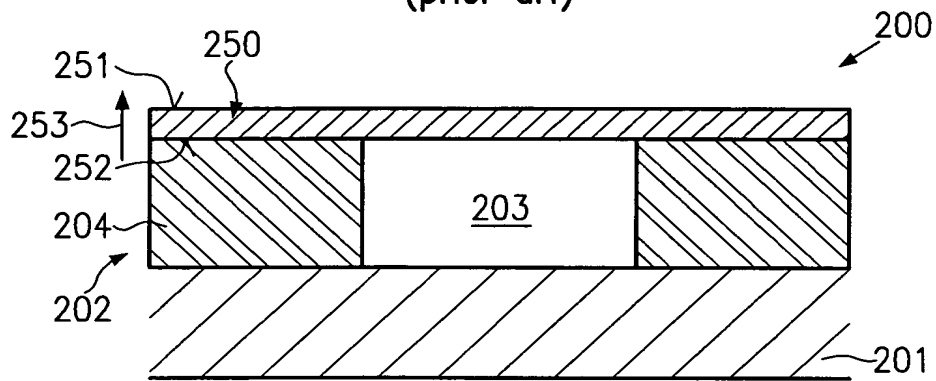


FIG. 2a

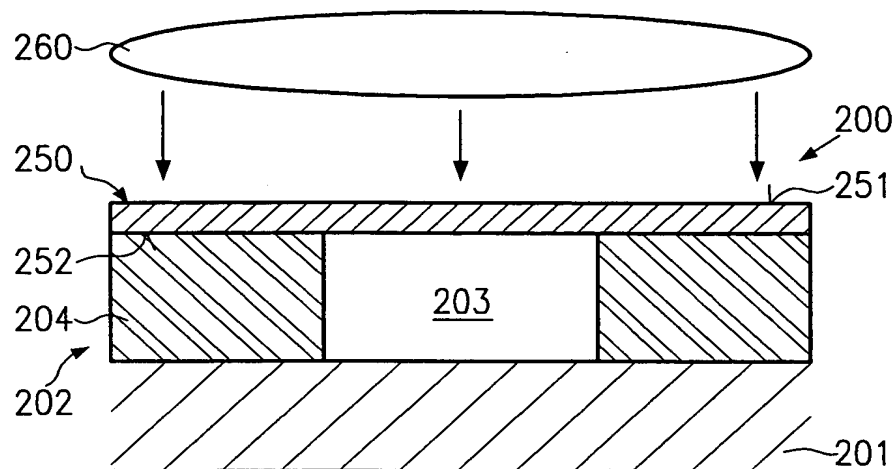


FIG. 2b

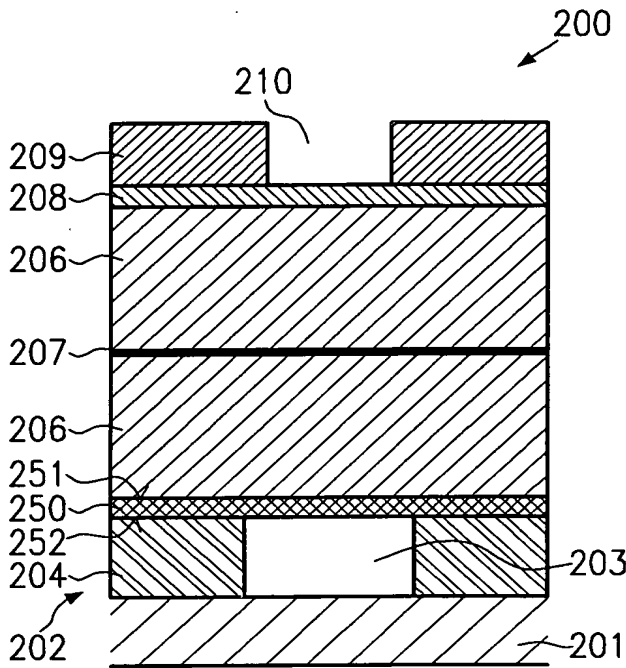


FIG. 2c

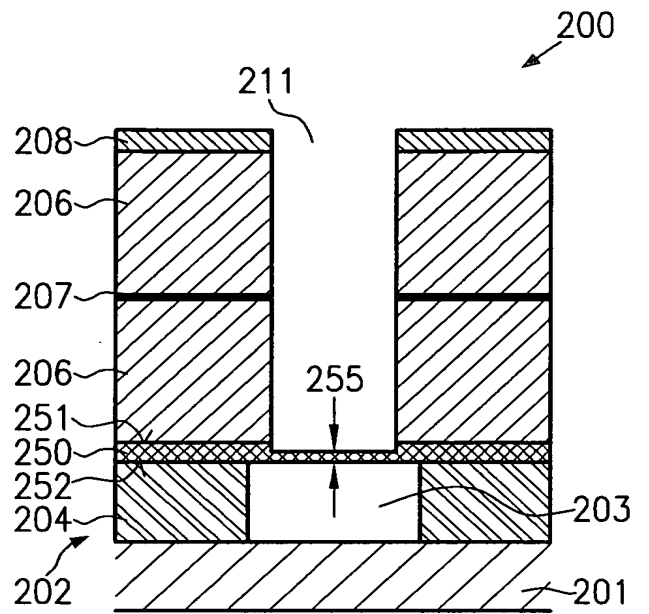


FIG. 2d

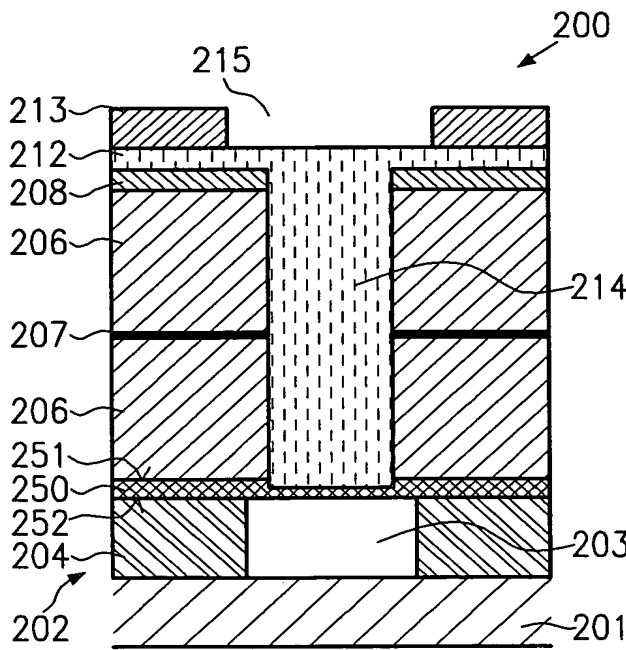


FIG. 2e

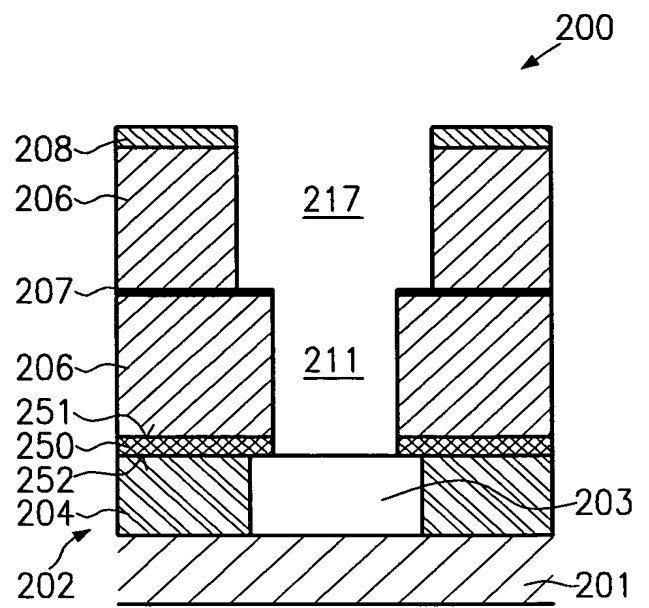


FIG. 2f

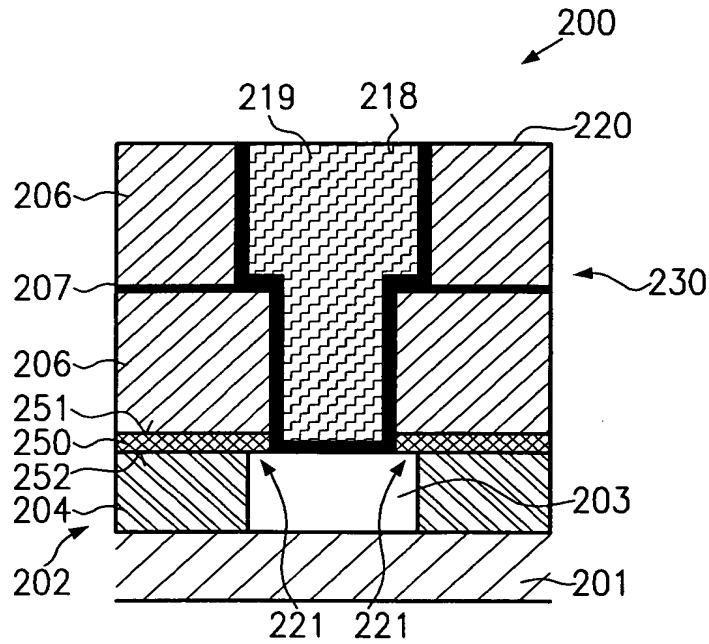


FIG. 2g